T209PCTUS

FIG. 1

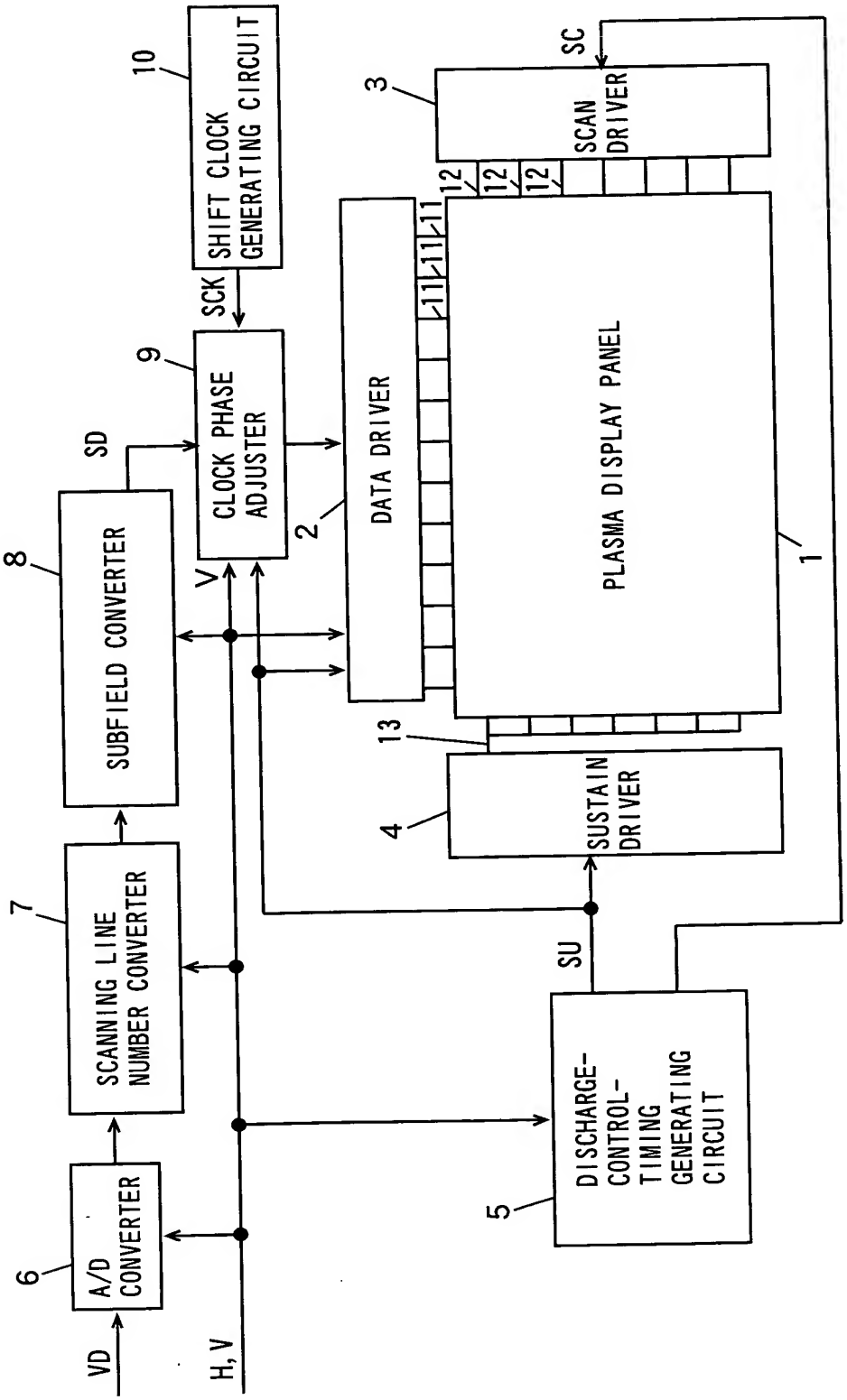


FIG. 2

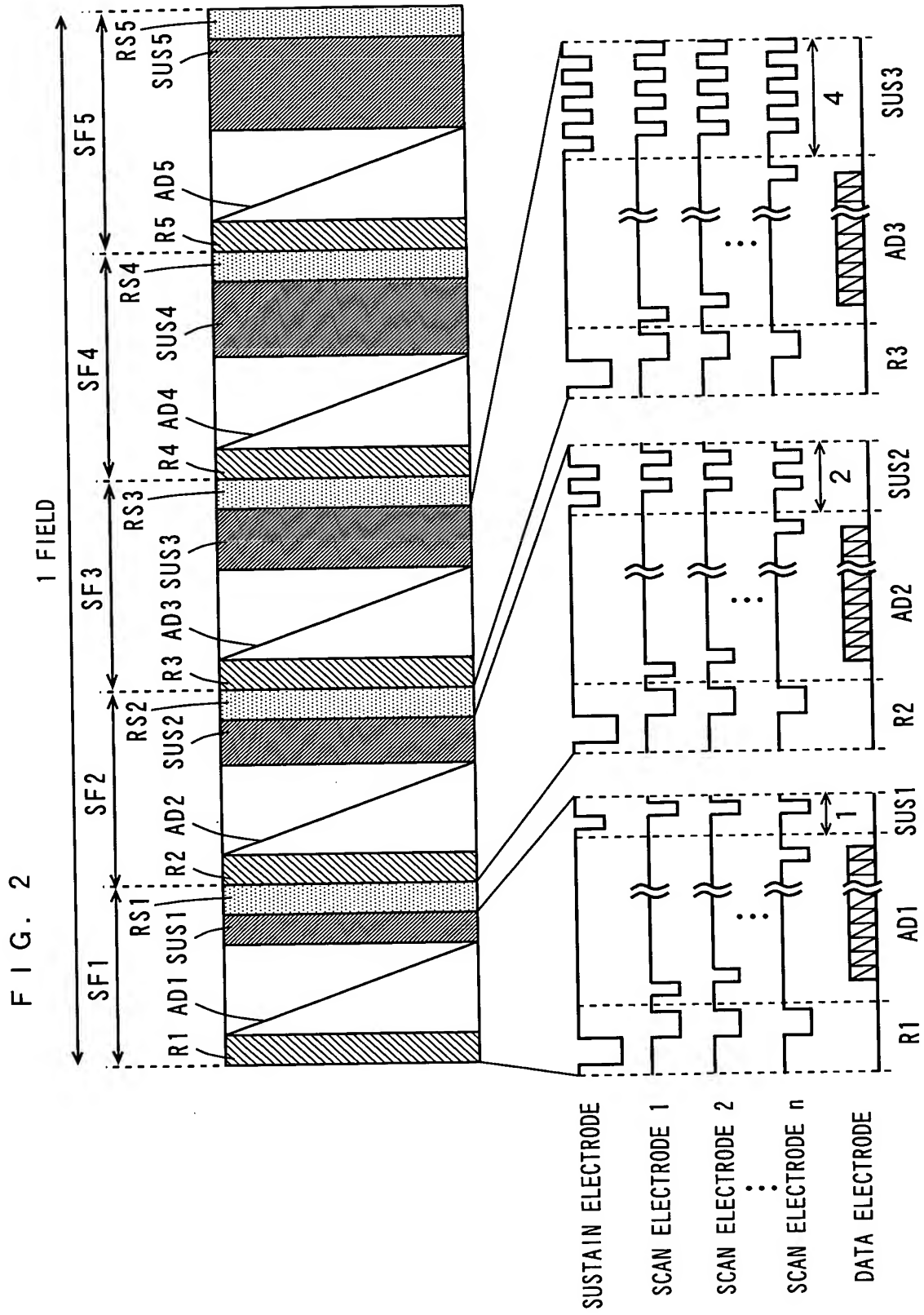

1 FIELD
SF1
SF2
SF3
SF4
SF5
R1
AD1
SUS1
RS1
R2
AD2
SUS2
RS2
R3
AD3
SUS3
RS3
R4
AD4
SUS4
RS4
R5
AD5
SUS5
RS5
SUSTAIN ELECTRODE
SCAN ELECTRODE 1
SCAN ELECTRODE 2
SCAN ELECTRODE n
DATA ELECTRODE
R1
AD1
SUS1
1
R2
AD2
SUS2
2
R3
AD3
SUS3
4

FIG. 3

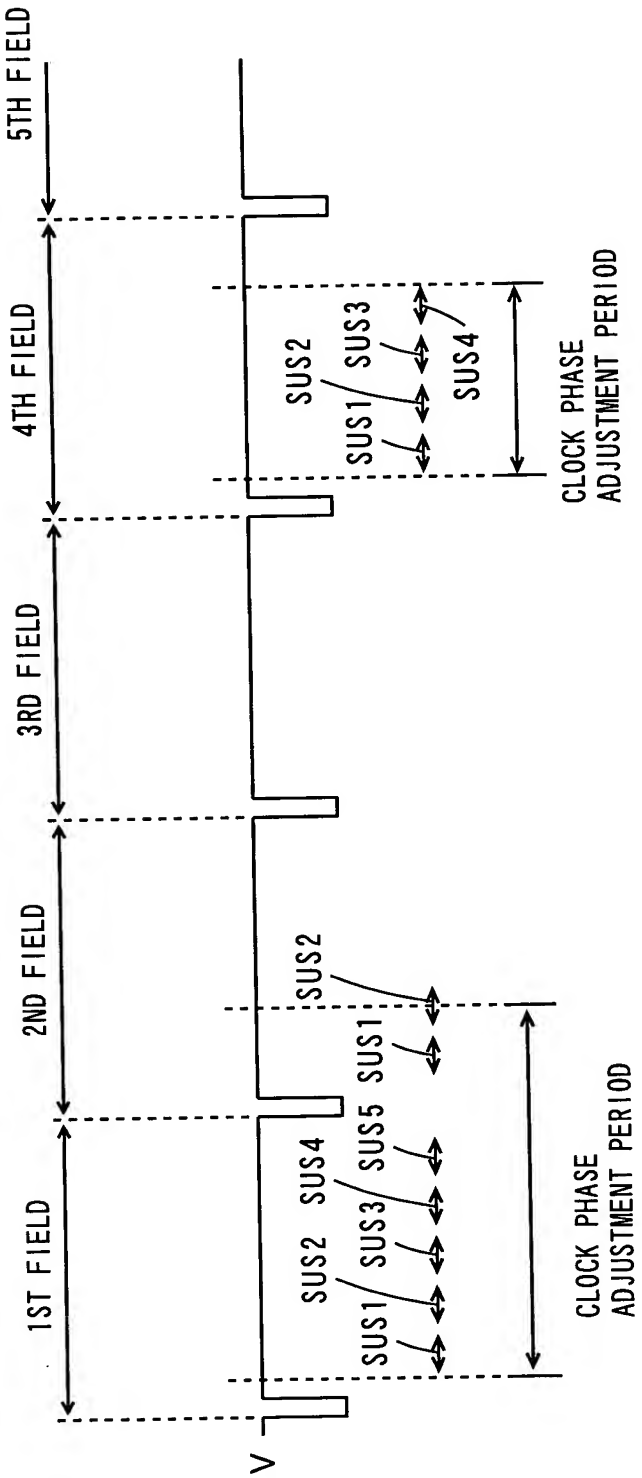

5TH FIELD
4TH FIELD
3RD FIELD
2ND FIELD
1ST FIELD
V
SUS2
SUS1
SUS3
SUS4
CLOCK PHASE ADJUSTMENT PERIOD
SUS2
SUS1
SUS5
SUS3
SUS4
CLOCK PHASE ADJUSTMENT PERIOD

FIG. 4

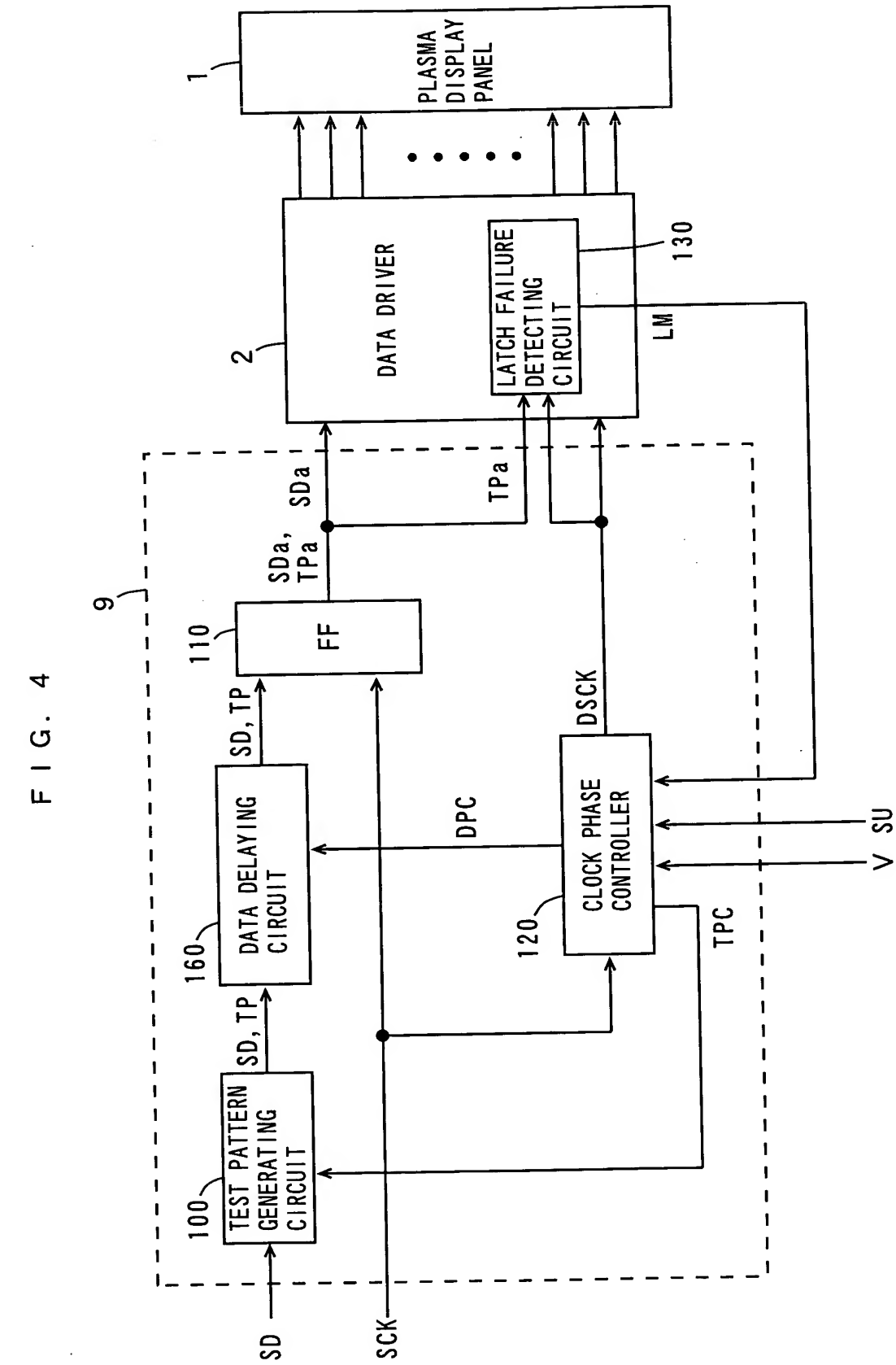

1
PLASMA DISPLAY PANEL
2
DATA DRIVER
LATCH FAILURE DETECTING CIRCUIT
130
LM
9
SDa
TPa
SDa, TPa
110
FF
SD, TP
160
DATA DELAYING CIRCUIT
DPC
DSCK
120
CLOCK PHASE CONTROLLER
V SU
TPC
SD, TP
100
TEST PATTERN GENERATING CIRCUIT
SD
SCK

FIG. 5

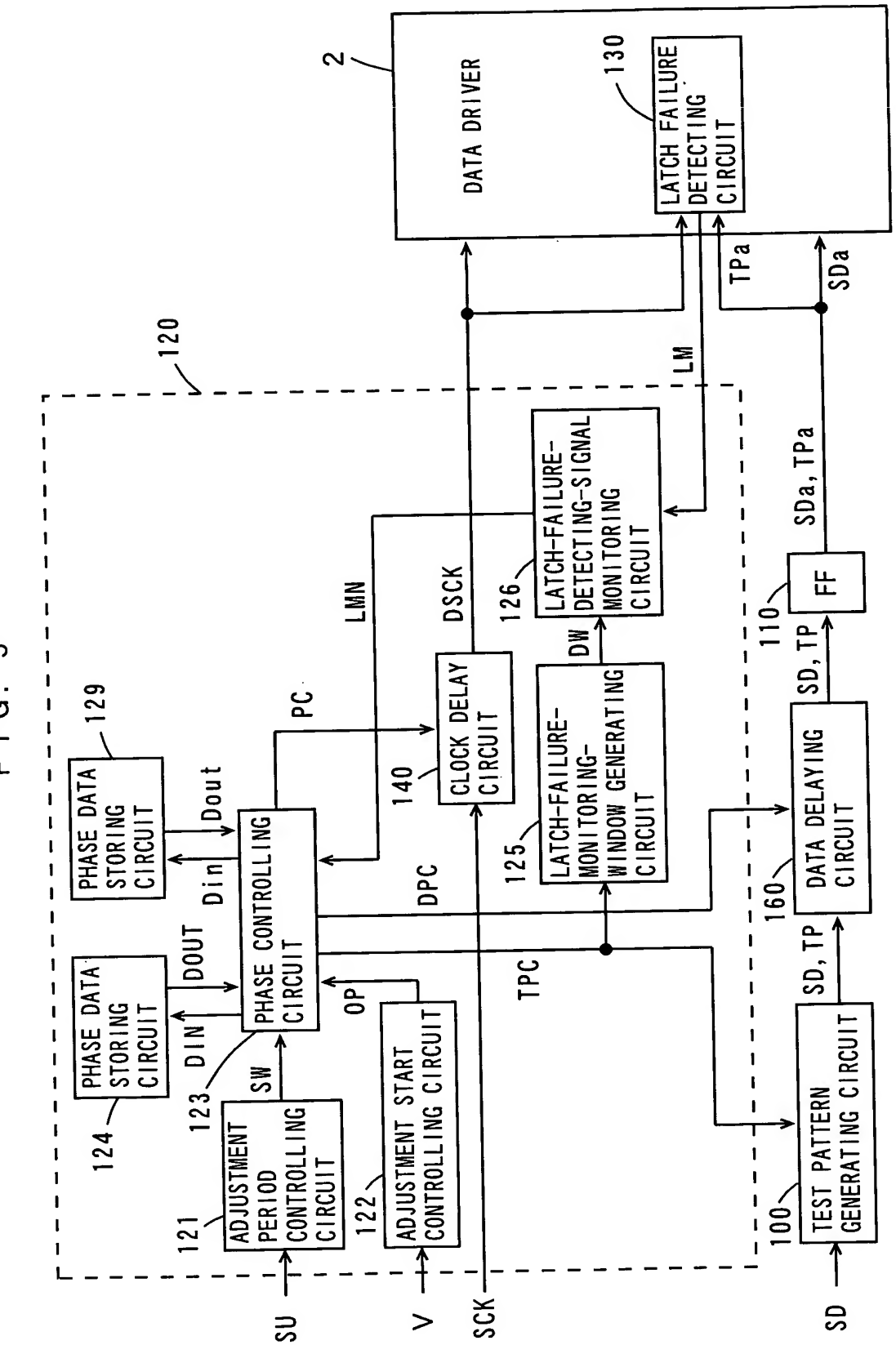

2
DATA DRIVER
130
LATCH FAILURE DETECTING CIRCUIT
120
LM
TPa
SDa
SDa, TPa
LMN
DSCK
126
LATCH-FAILURE-DETECTING-SIGNAL MONITORING CIRCUIT
DW
110
FF
SD, TP
160
DATA DELAYING CIRCUIT
PC
140
CLOCK DELAY CIRCUIT
DPC
125
LATCH-FAILURE-MONITORING-WINDOW GENERATING CIRCUIT
TPC
129
PHASE DATA STORING CIRCUIT
Dout
Din
DOUT
DIN
PHASE CONTROLLING CIRCUIT
123
SW
OP
124
PHASE DATA STORING CIRCUIT
121
ADJUSTMENT PERIOD CONTROLLING CIRCUIT
122
ADJUSTMENT START CONTROLLING CIRCUIT
100
TEST PATTERN GENERATING CIRCUIT
SU
V
SCK
SD

FIG. 6

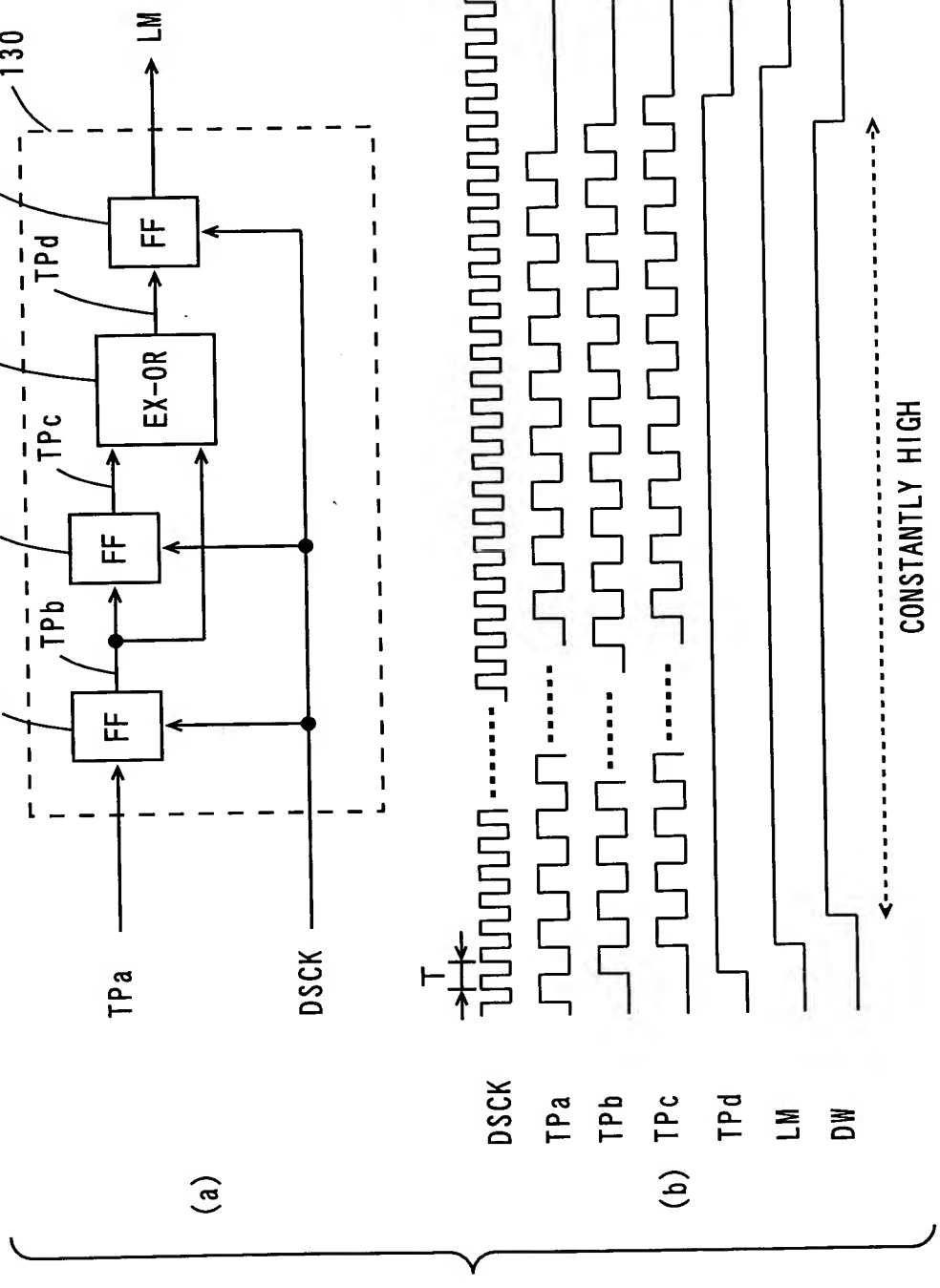

(a)
130
131
132
133
134
FF
FF
EX-OR
FF
TPa
TPb
TPc
TPd
DSCK
LM
(b)
T
DSCK
TPa
TPb
TPc
TPd
LM
DW
CONSTANTLY HIGH

FIG. 7

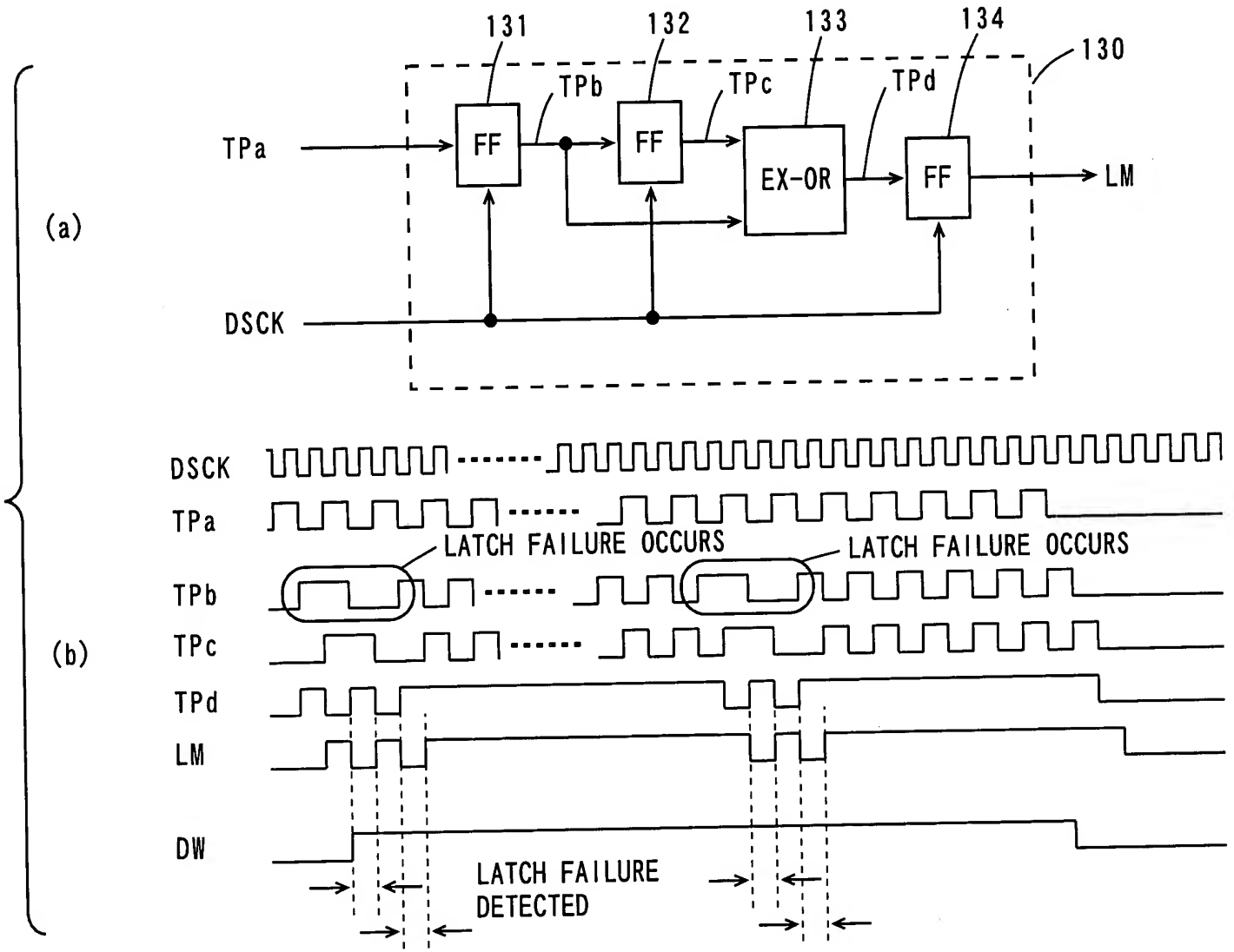
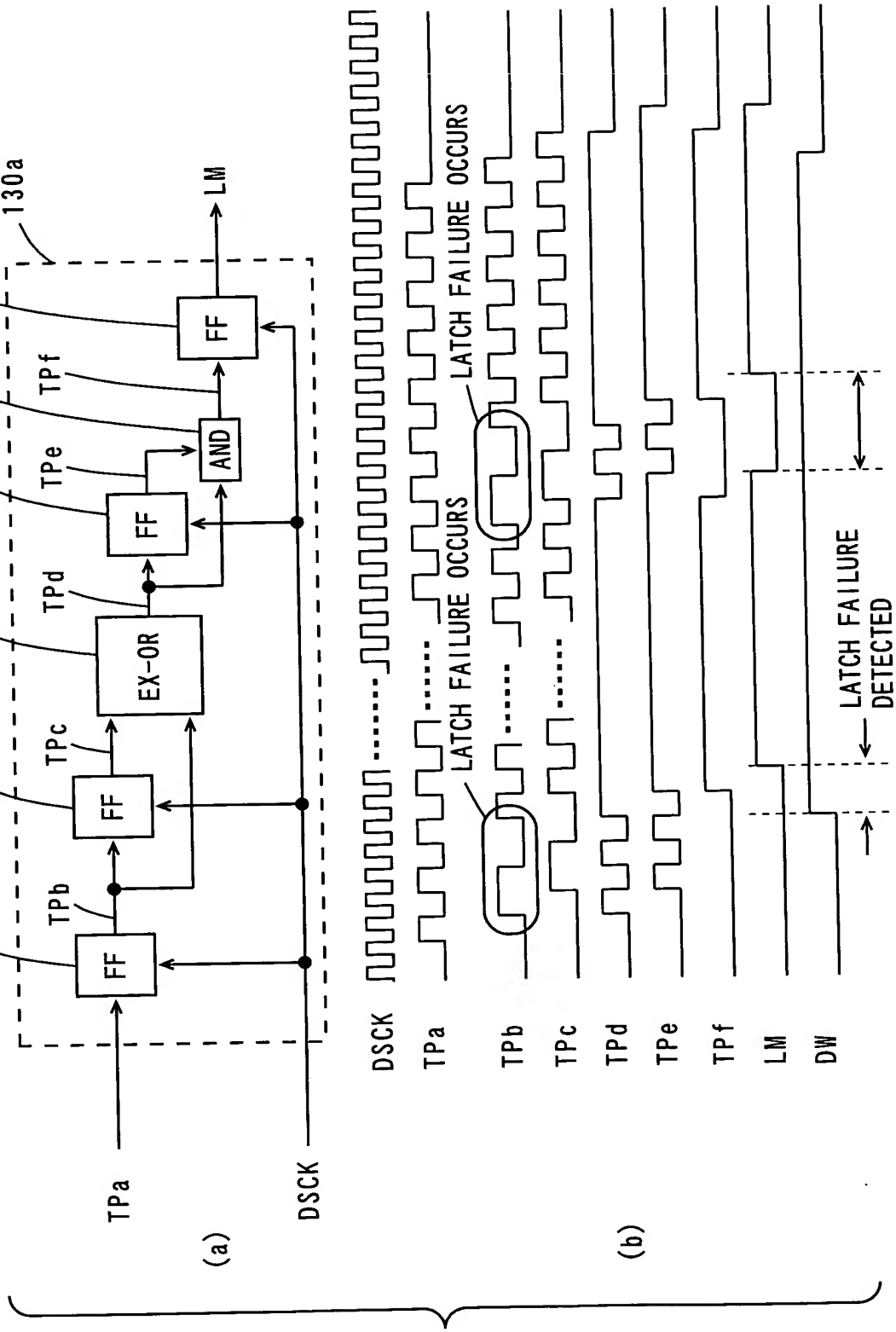

(a)
131
132
133
134
130
TPa
TPb
TPc
TPd
FF
FF
EX-OR
FF
LM
DSCK
(b)
DSCK
TPa
LATCH FAILURE OCCURS
LATCH FAILURE OCCURS
TPb
TPc
TPd
LM
DW
LATCH FAILURE
DETECTED

FIG. 8


130a
131
132
133
134
135
136
FF
FF
EX-OR
FF
AND
FF
TPa
TPb
TPc
TPd
TPe
TPf
LM
DSCK
(a)
DSCK
TPa
TPb
TPc
TPd
TPe
TPf
LM
DW
LATCH FAILURE OCCURS
LATCH FAILURE OCCURS
LATCH FAILURE DETECTED
(b)

F I G. 9

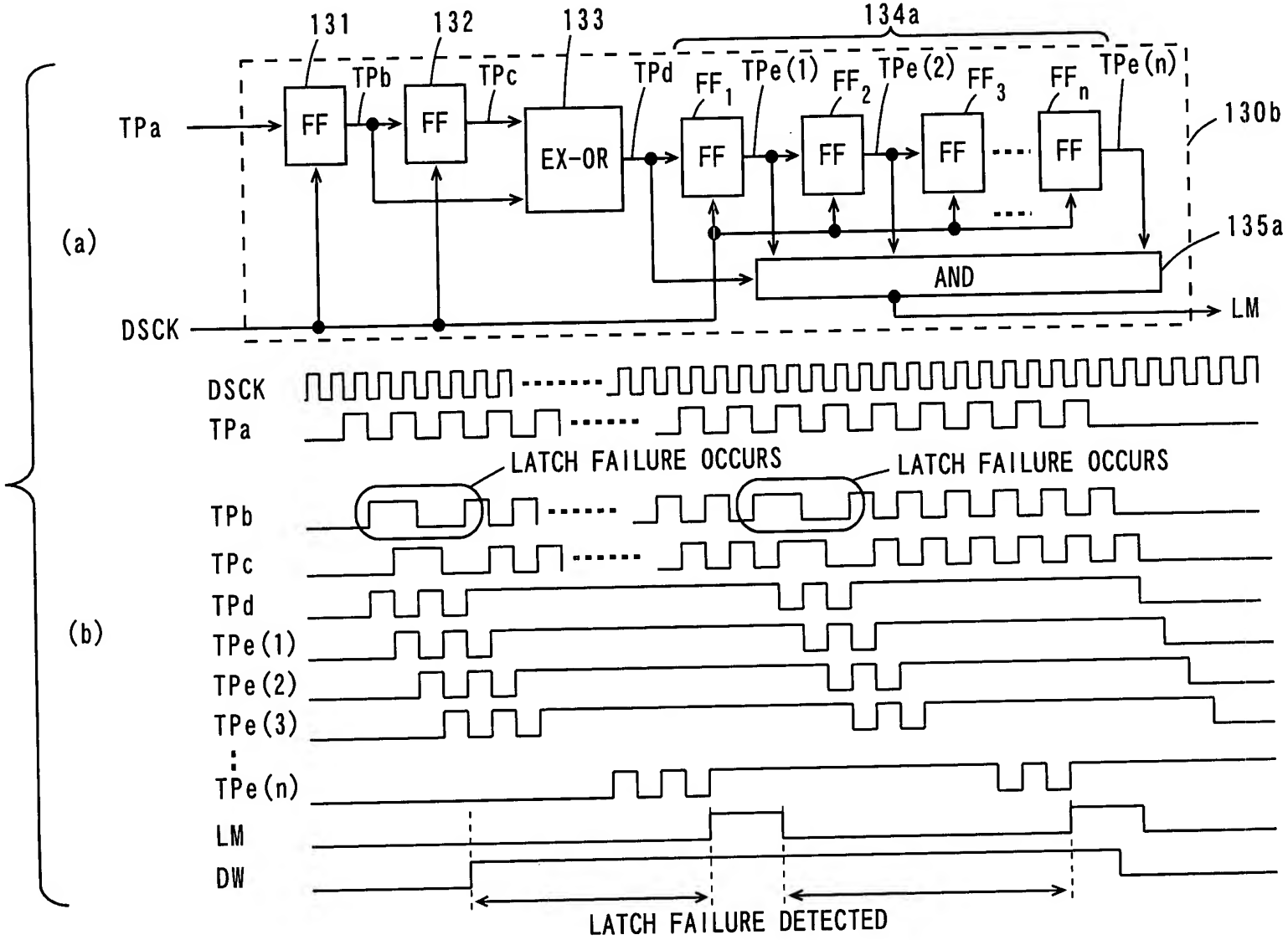

131
132
133
134a
TPa
TPb
TPc
TPd
FF1
TPe(1)
FF2
TPe(2)
FF3
FFn
TPe(n)
FF
EX-OR
130b
(a)
135a
AND
DSCK
LM
DSCK
TPa
LATCH FAILURE OCCURS
LATCH FAILURE OCCURS
TPb
TPc
TPd
(b)
TPe(1)
TPe(2)
TPe(3)
TPe(n)
LM
DW
LATCH FAILURE DETECTED

FIG. 10

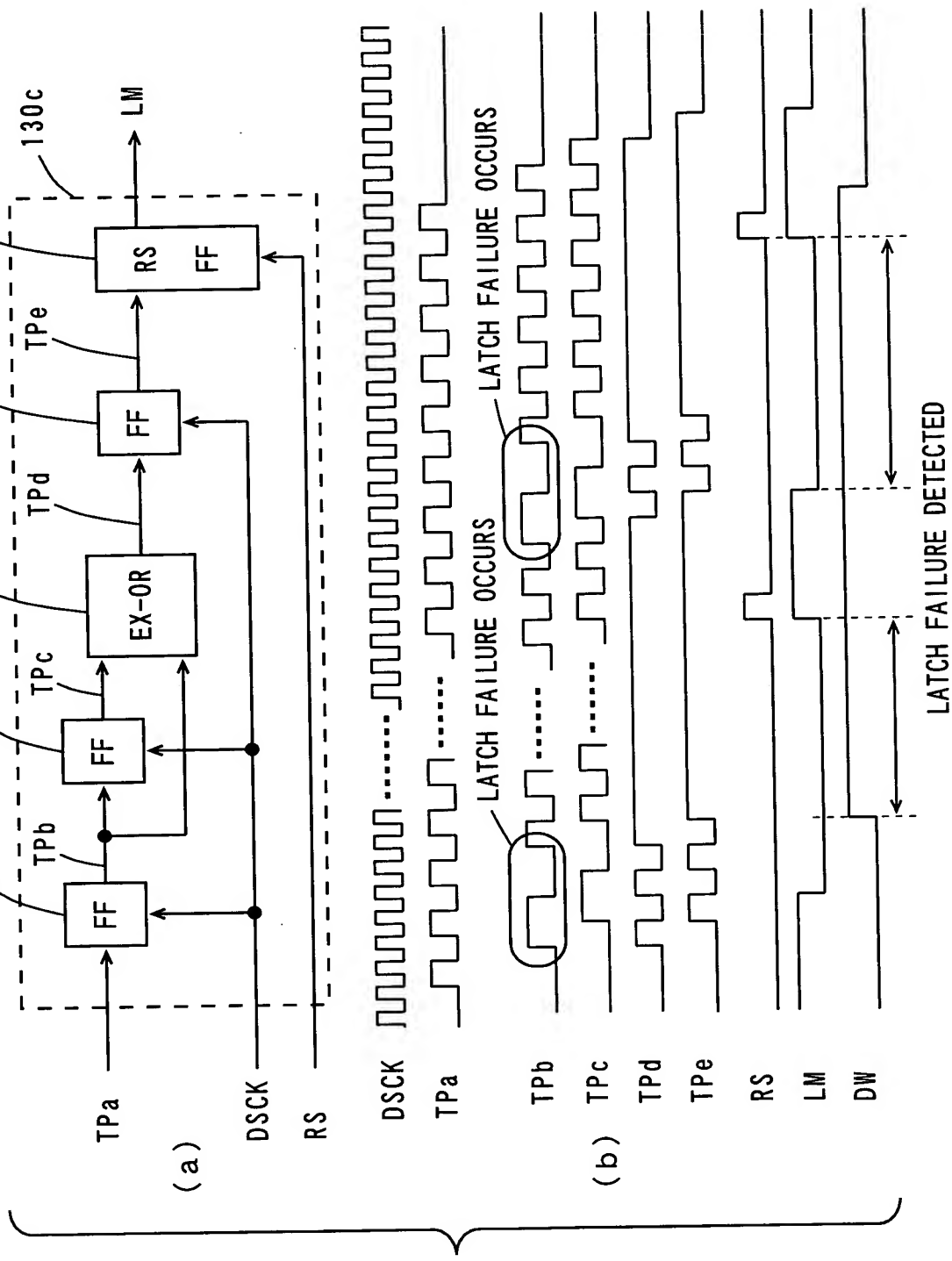

(a)
TPa
DSCK
RS
131
FF
TPb
132
FF
TPc
133
EX-OR
TPd
134
FF
TPe
137
RS
FF
LM
130c
(b)
DSCK
TPa
LATCH FAILURE OCCURS
TPb
TPc
TPd
TPe
RS
LM
DW
LATCH FAILURE OCCURS
LATCH FAILURE DETECTED

FIG. 11

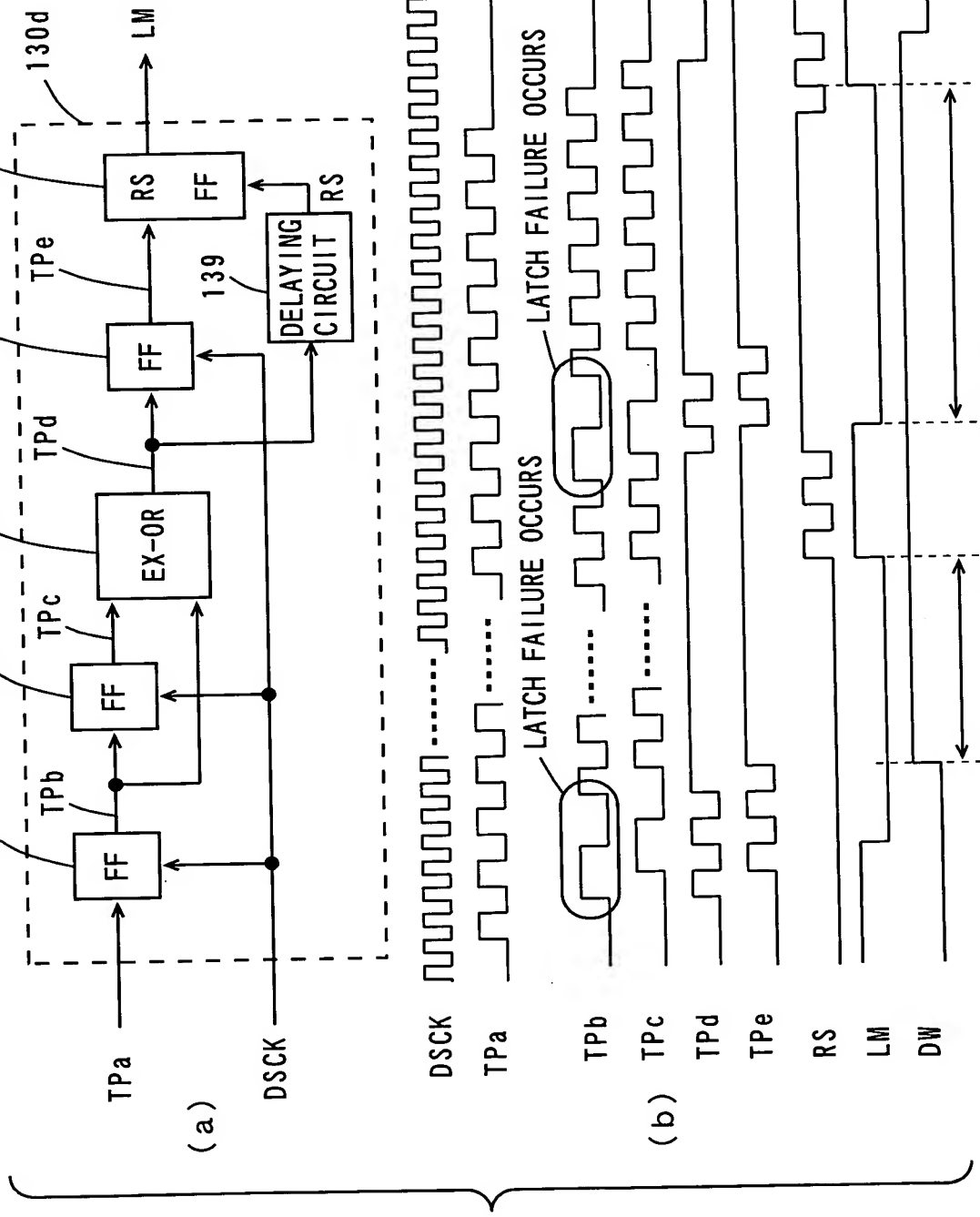

(a)
TPa
DSCK
131
FF
TPb
132
FF
TPc
133
EX-OR
TPd
134
FF
TPe
139
DELAYING CIRCUIT
RS
137
RS FF
LM
130d
(b)
DSCK
TPa
LATCH FAILURE OCCURS
LATCH FAILURE OCCURS
TPb
TPc
TPd
TPe
RS
LM
DW
LATCH FAILURE DETECTED

FIG. 12

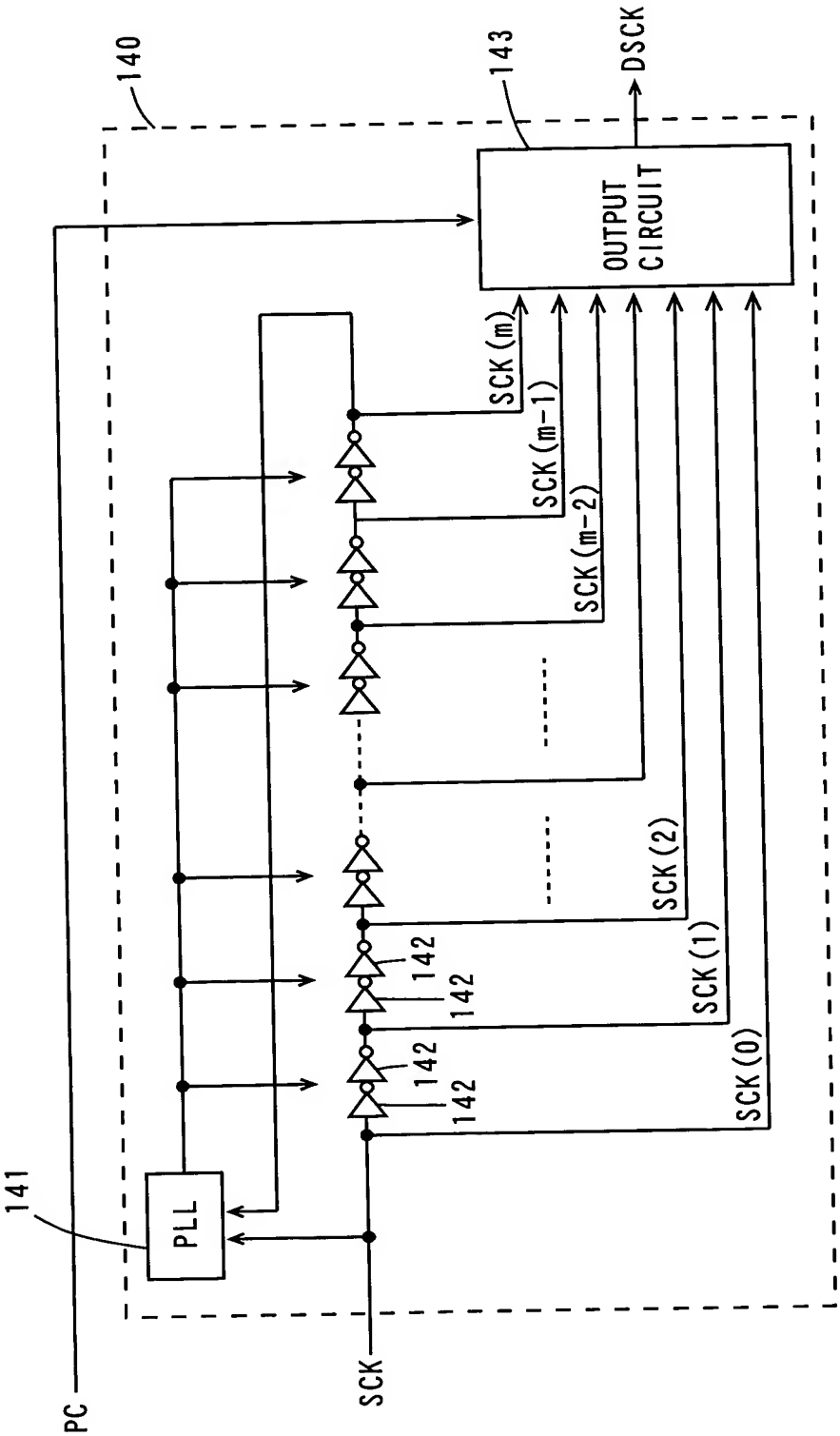

140
143
DSCK
OUTPUT CIRCUIT
SCK (m)
SCK (m-1)
SCK (m-2)
SCK (2)
SCK (1)
SCK (0)
142
142
142
142
141
PLL
PC
SCK

FIG. 13

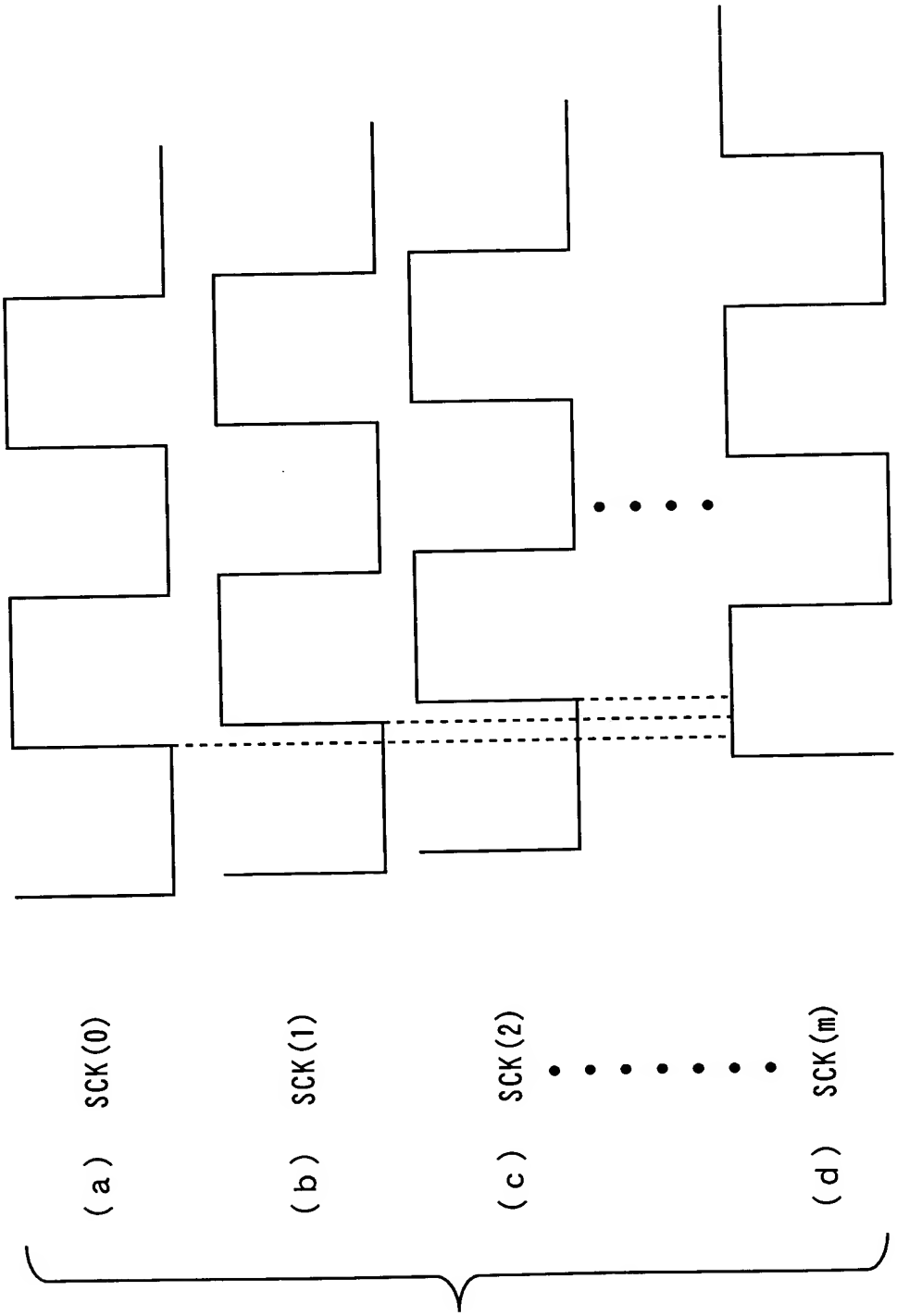


FIG. 14

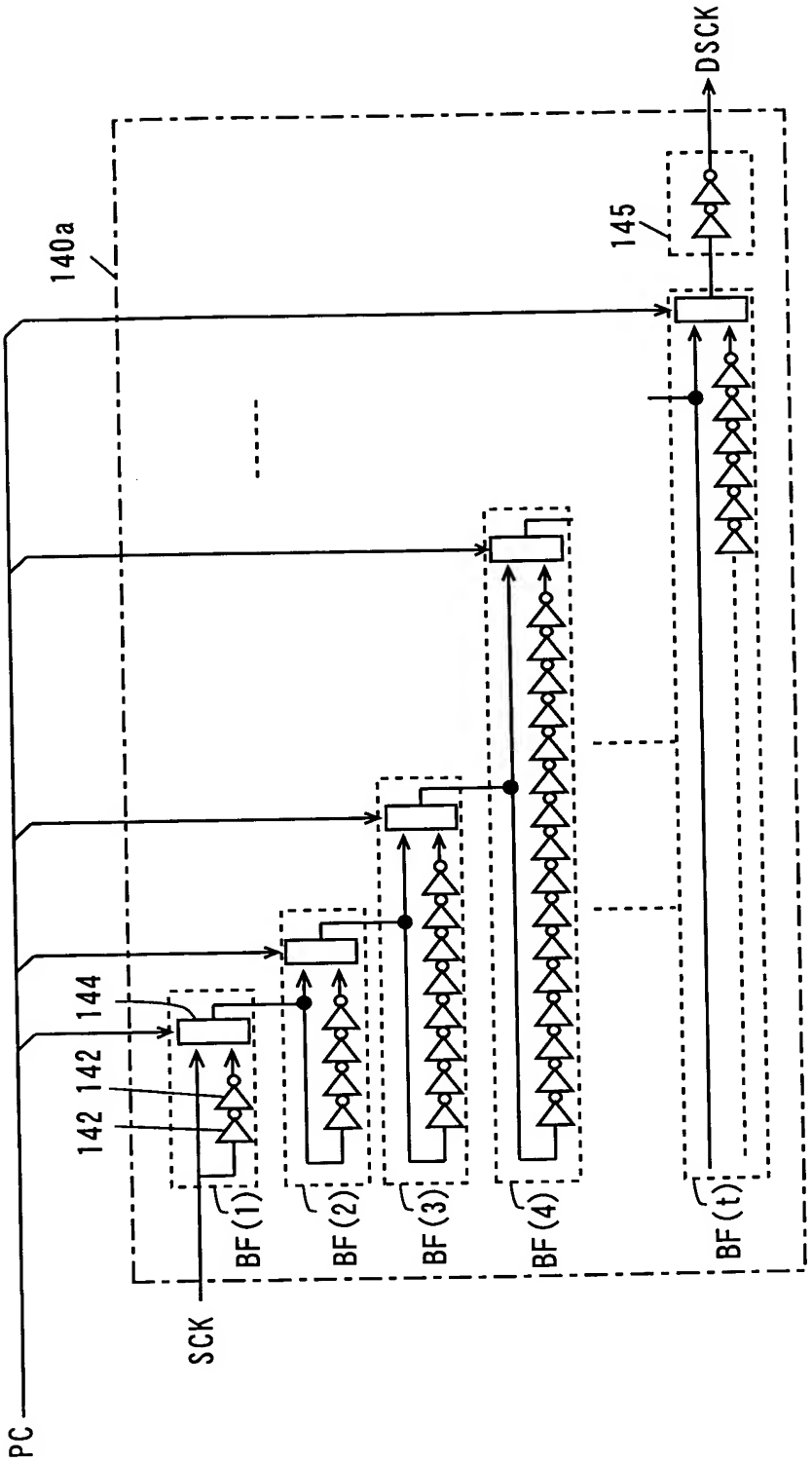
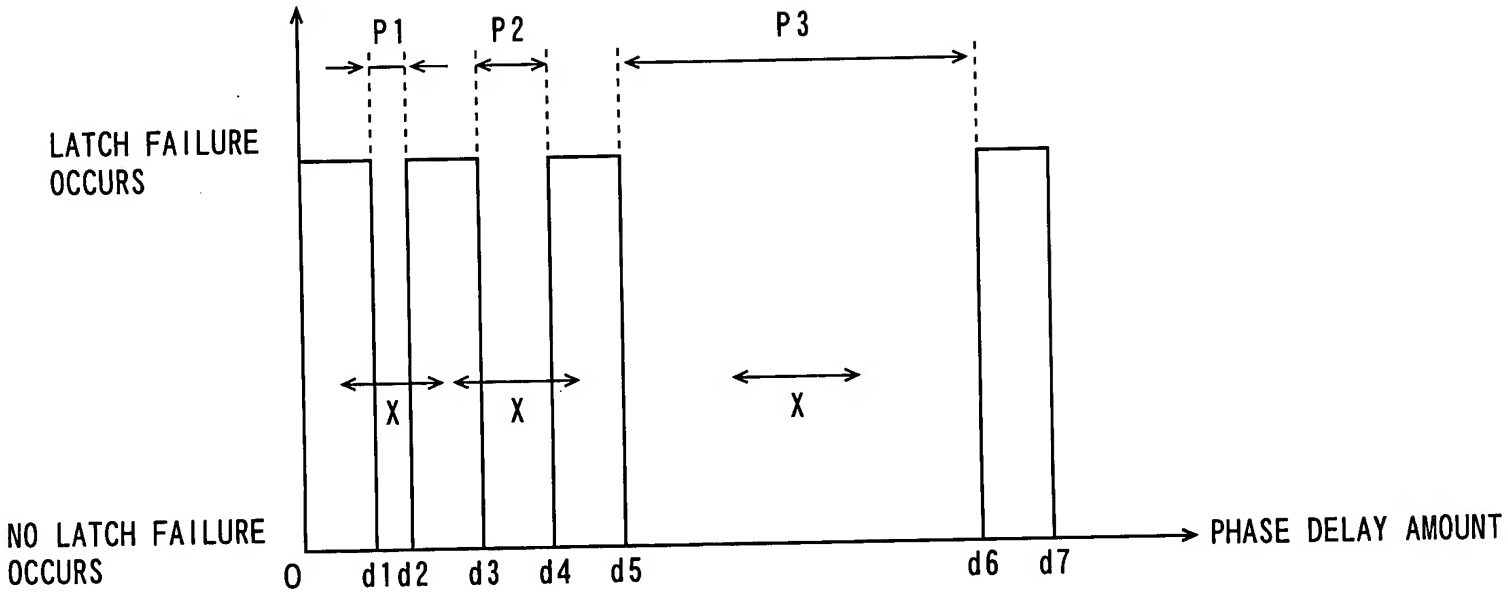


FIG. 15



P1<THRESHOLD X
P2<THRESHOLD X
P3>THRESHOLD X ⇒ OPTIMAL PHASE DELAY AMOUNT $= \frac{d5+d6}{2}$

FIG. 16

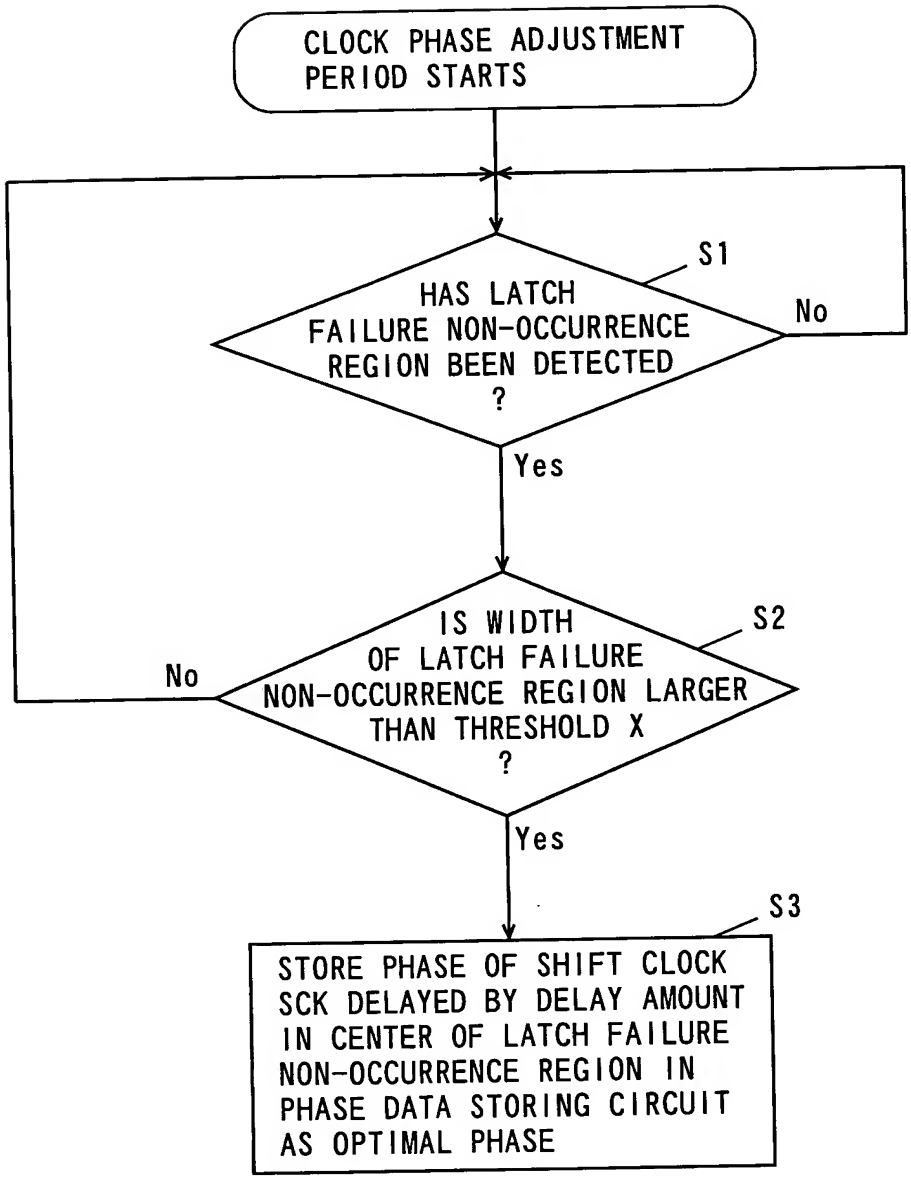

CLOCK PHASE ADJUSTMENT PERIOD STARTS
S1
HAS LATCH FAILURE NON-OCCURRENCE REGION BEEN DETECTED ?
No
Yes
S2
IS WIDTH OF LATCH FAILURE NON-OCCURRENCE REGION LARGER THAN THRESHOLD X ?
No
Yes
S3
STORE PHASE OF SHIFT CLOCK SCK DELAYED BY DELAY AMOUNT IN CENTER OF LATCH FAILURE NON-OCCURRENCE REGION IN PHASE DATA STORING CIRCUIT AS OPTIMAL PHASE

FIG. 17

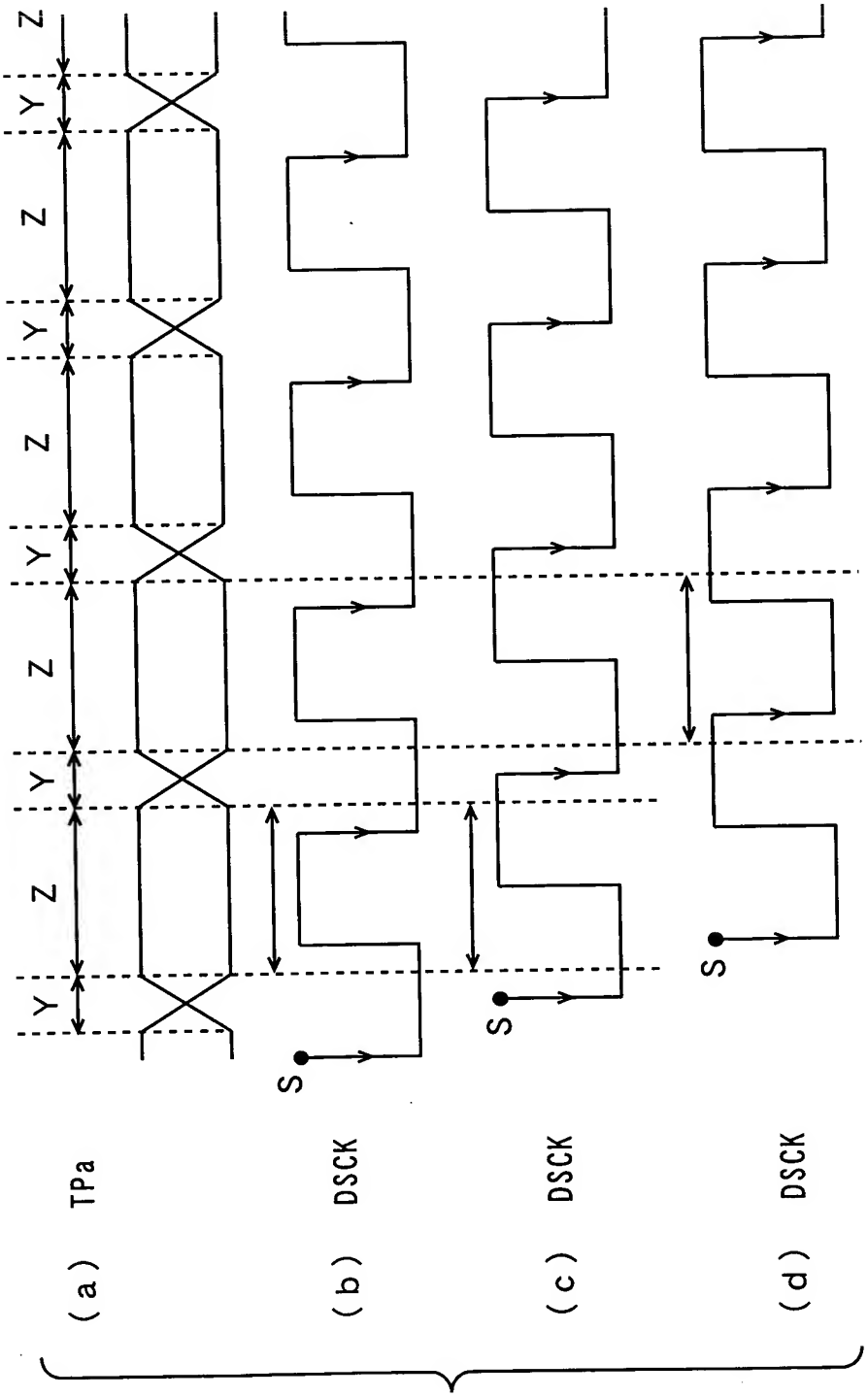


FIG. 18

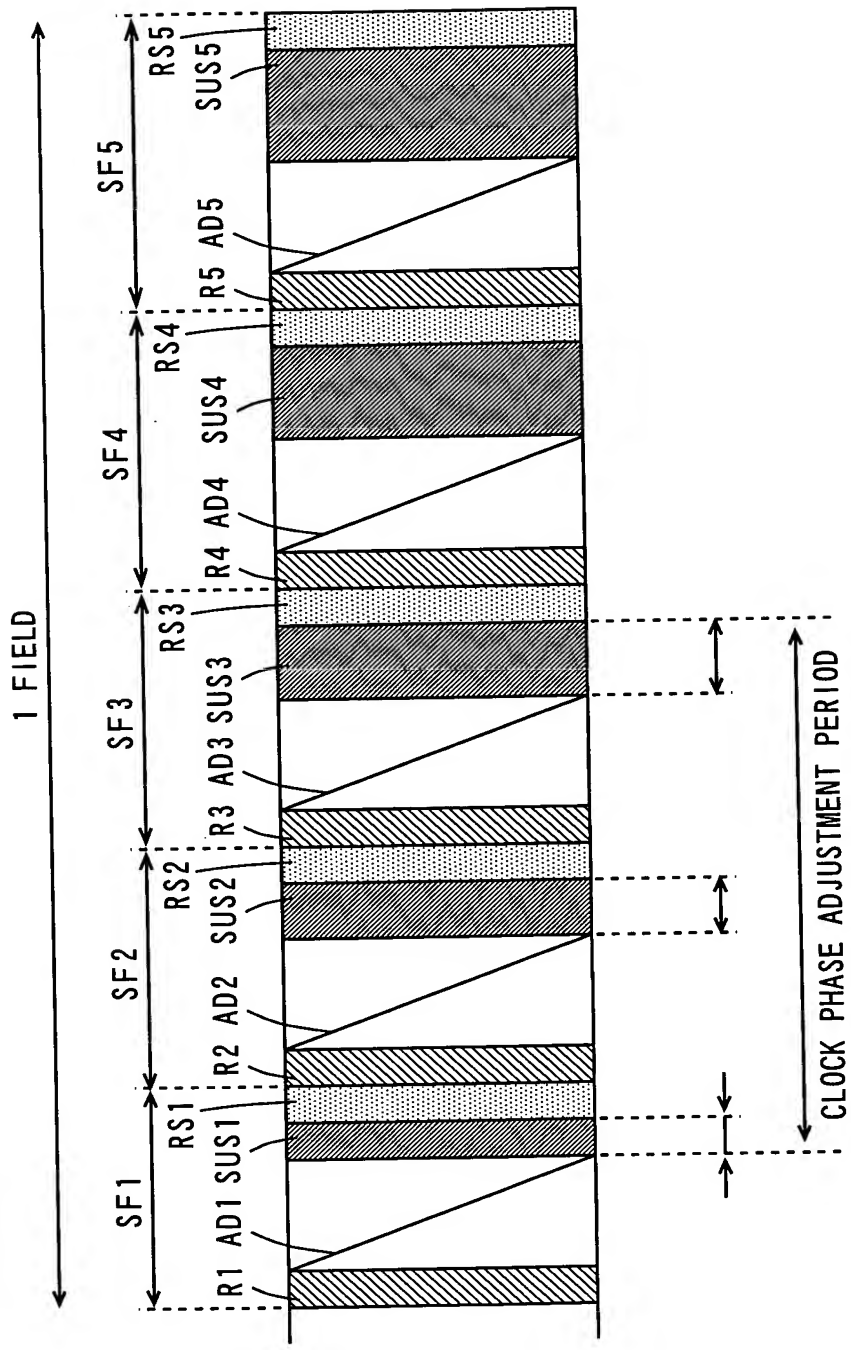

1 FIELD
SF1
SF2
SF3
SF4
SF5
R1
AD1
SUS1
RS1
R2
AD2
SUS2
RS2
R3
AD3
SUS3
RS3
R4
AD4
SUS4
RS4
R5
AD5
SUS5
RS5
CLOCK PHASE ADJUSTMENT PERIOD

FIG. 19

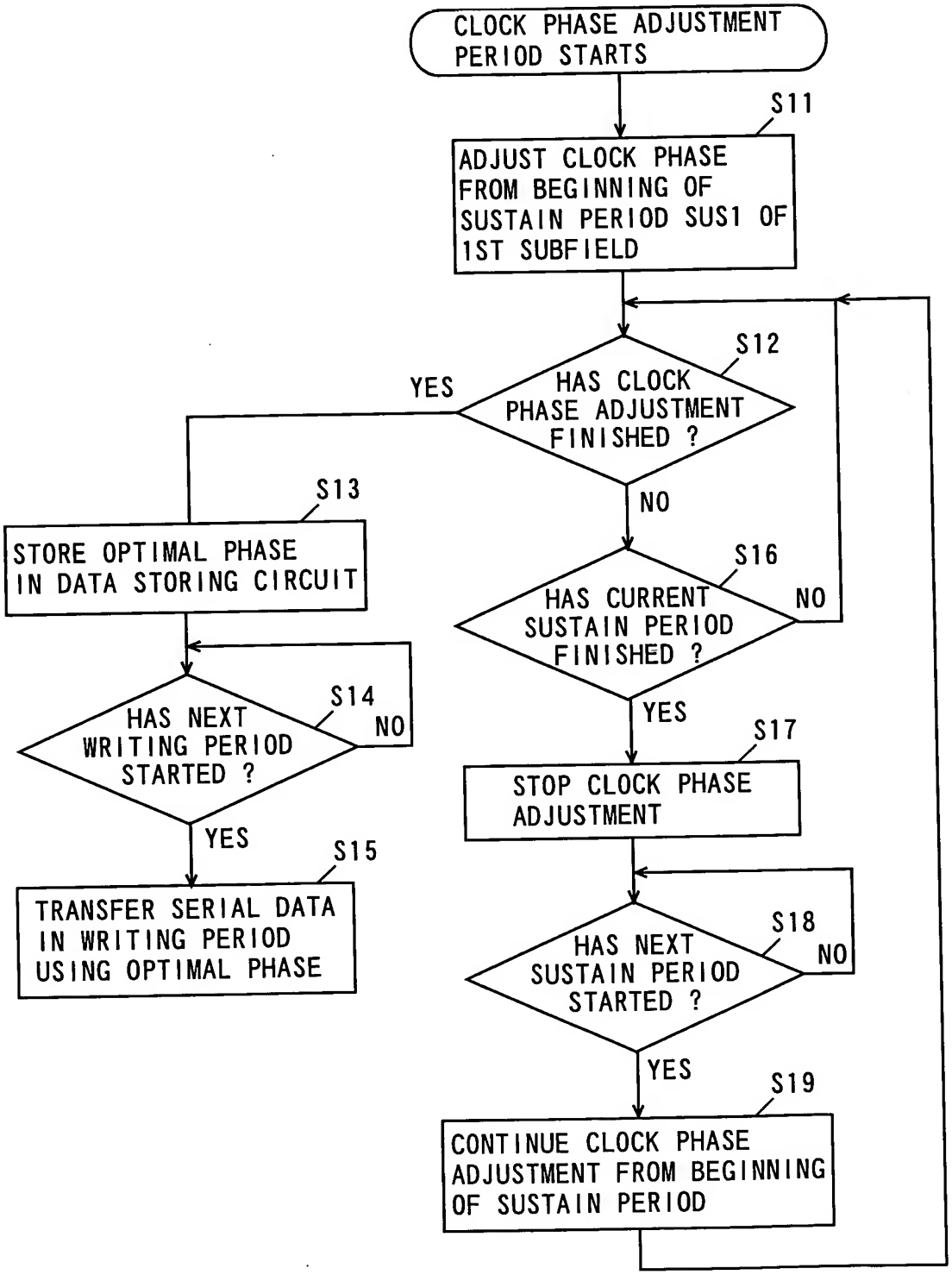

CLOCK PHASE ADJUSTMENT PERIOD STARTS
S11
ADJUST CLOCK PHASE FROM BEGINNING OF SUSTAIN PERIOD SUS1 OF 1ST SUBFIELD
S12
HAS CLOCK PHASE ADJUSTMENT FINISHED ?
YES
NO
S13
STORE OPTIMAL PHASE IN DATA STORING CIRCUIT
S14
HAS NEXT WRITING PERIOD STARTED ?
NO
YES
S15
TRANSFER SERIAL DATA IN WRITING PERIOD USING OPTIMAL PHASE
S16
HAS CURRENT SUSTAIN PERIOD FINISHED ?
NO
YES
S17
STOP CLOCK PHASE ADJUSTMENT
S18
HAS NEXT SUSTAIN PERIOD STARTED ?
NO
YES
S19
CONTINUE CLOCK PHASE ADJUSTMENT FROM BEGINNING OF SUSTAIN PERIOD

FIG. 20

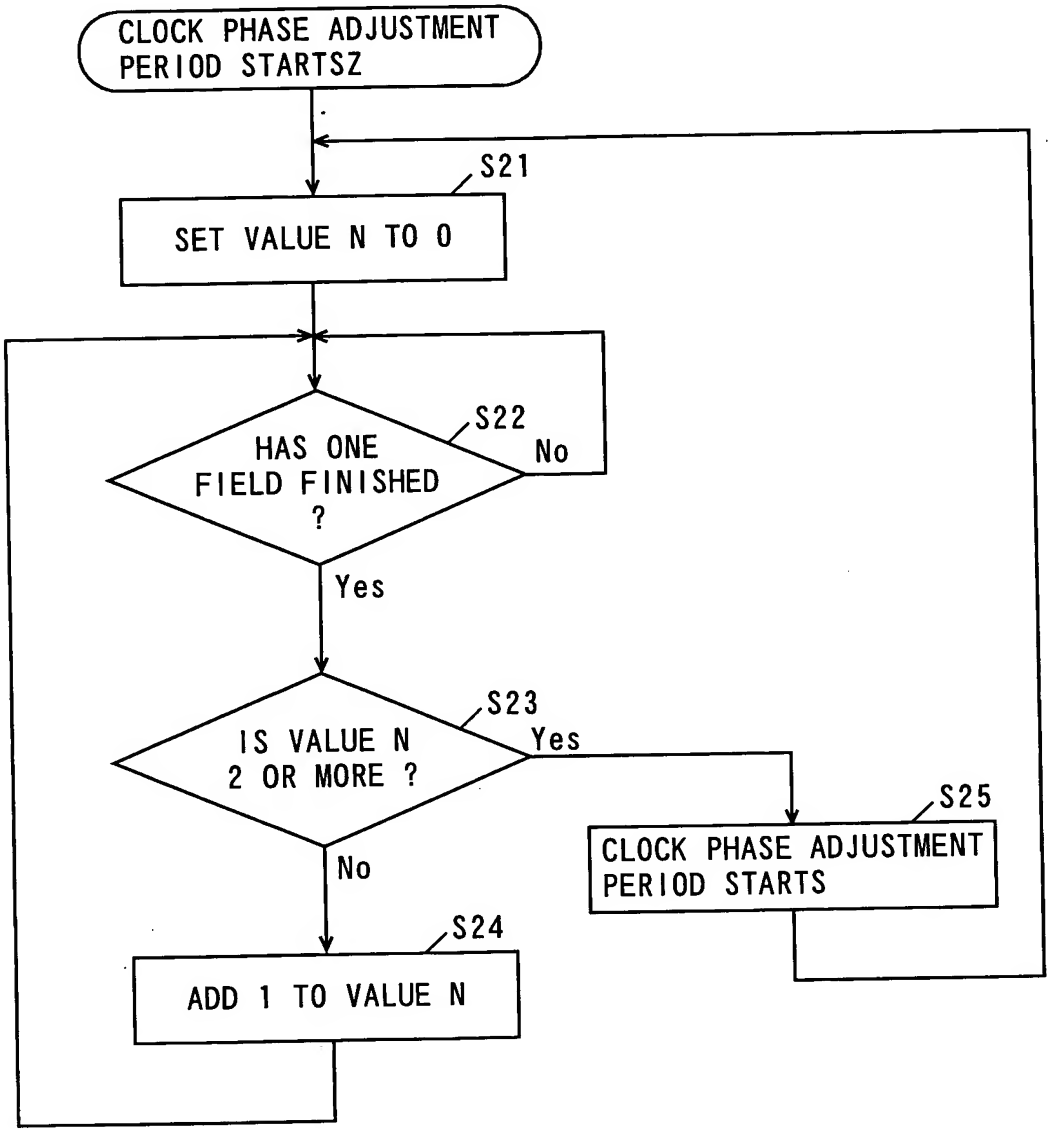
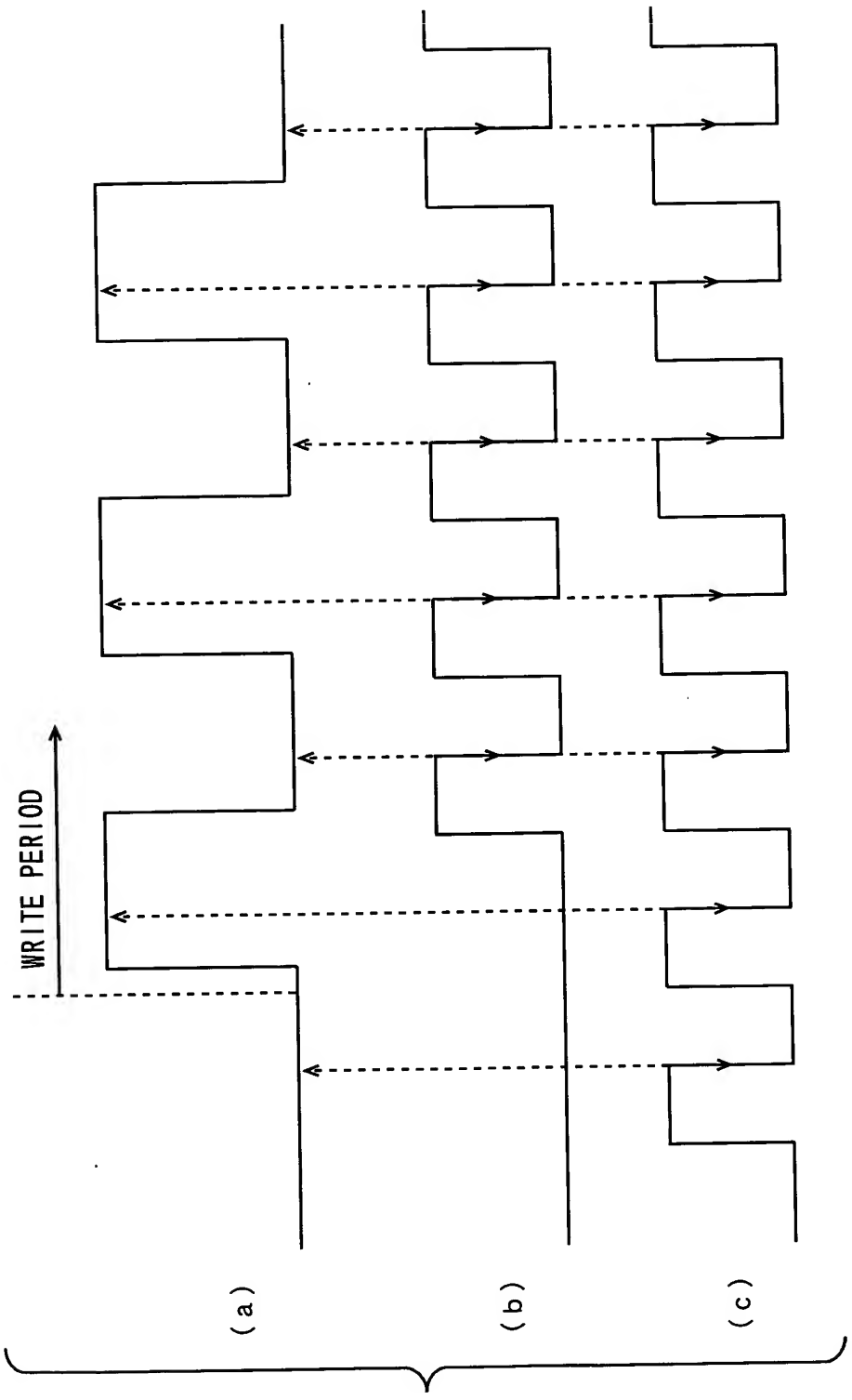

CLOCK PHASE ADJUSTMENT PERIOD STARTSZ
S21
SET VALUE N TO 0
S22
HAS ONE FIELD FINISHED ?
No
Yes
S23
IS VALUE N 2 OR MORE ?
Yes
No
S25
CLOCK PHASE ADJUSTMENT PERIOD STARTS
S24
ADD 1 TO VALUE N

FIG. 21



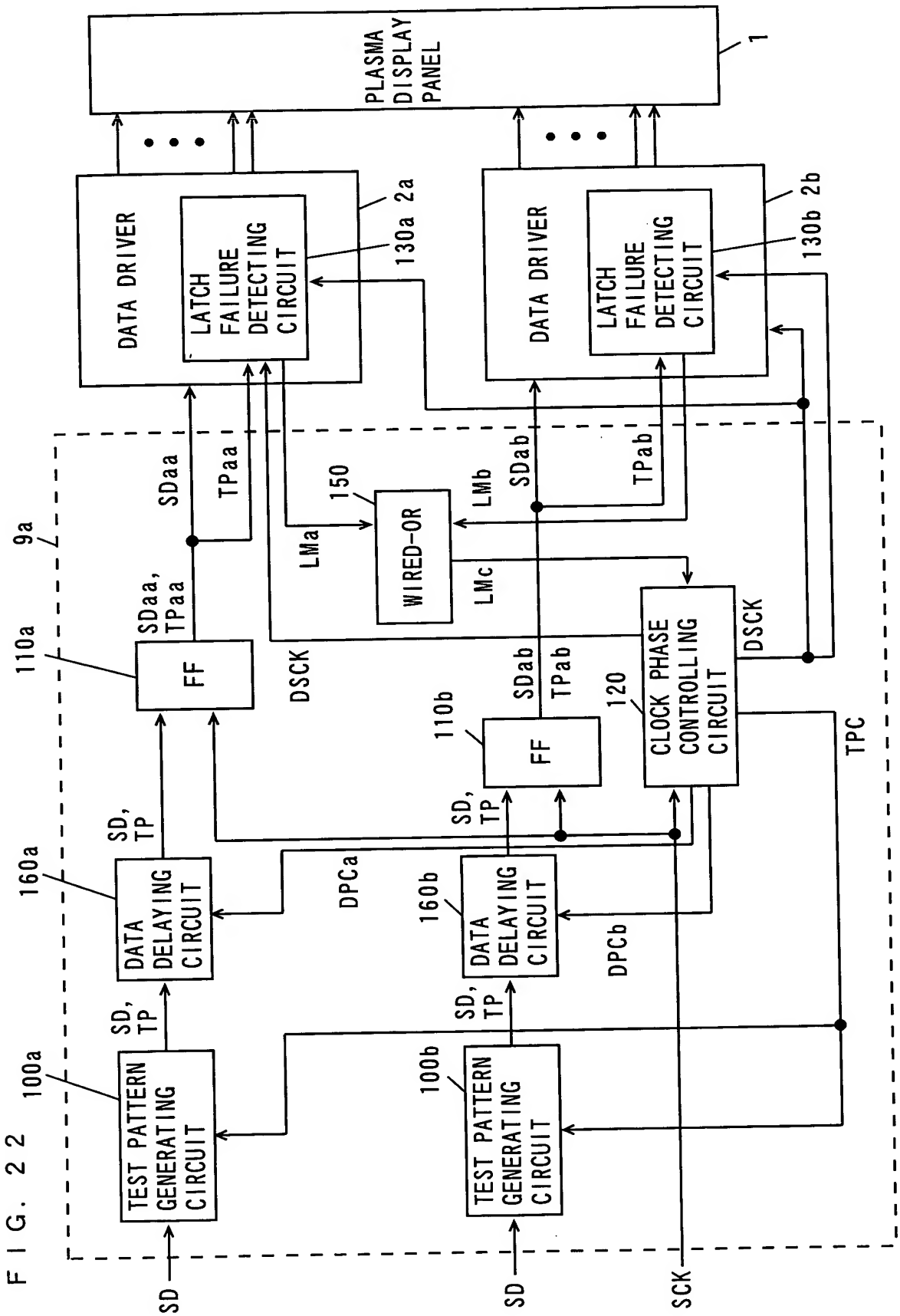

PLASMA DISPLAY PANEL
1
DATA DRIVER
LATCH FAILURE DETECTING CIRCUIT
130a 2a
DATA DRIVER
LATCH FAILURE DETECTING CIRCUIT
130b 2b
9a
SDaa
TPaa
150
WIRED-OR
LMa
LMb
LMc
SDab
TPab
SDaa, TPaa
110a
FF
DSCK
SDab
TPab
110b
FF
120
CLOCK PHASE CONTROLLING CIRCUIT
DSCK
TPC
SD, TP
160a
DATA DELAYING CIRCUIT
DPCa
160b
DATA DELAYING CIRCUIT
DPCb
SD, TP
100a
TEST PATTERN GENERATING CIRCUIT
100b
TEST PATTERN GENERATING CIRCUIT
SD
SD
SCK

FIG. 22